AMENDMENTS TO THE CLAIMS:

Please amend claim 32 as follows.

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. *(Original)* A direct memory access controller for controlling data transfer between a data source and a data destination comprising:

a read/write port operable to receive data from said data source via a source bus and to output said received data to said data destination via a destination bus; wherein

said direct memory access controller is operable in response to a predetermined number of clock pulses, to control said read/write port to output said received data said predetermined number of clock pulses after having received it.

2. *(Original)* A direct memory access controller according to claim 1, wherein said predetermined number of clock pulses is one and said memory access controller comprises a register to store said received data during said one clock cycle prior to outputting said received data.

3. *(Original)* A direct memory access controller according to claim 1, wherein said predetermined number of clock pulses is one and said memory access controller

comprises two registers arranged in parallel to each other, each operable to store alternate items of said received data during a clock cycle prior to outputting said stored items.

4. *(Original)* A direct memory access controller according to claim 1, wherein said predetermined number of clock pulses is zero, and said input port is connected to said output port, such that said received data is not stored within said direct memory access controller.

5. *(Original)* A direct memory access controller according to claim 4, further comprising combinatorial logic between said input and said output port.

6. *(Original)* A direct memory access controller according to claim 1, wherein said predetermined number of clock pulses is two and said memory access controller comprises an input register and an output register to store said received data during said two clock cycles prior to outputting it.

7. *(Original)* A direct memory access controller according to claim 1, wherein said source bus and said destination bus comprise a single bus, said single bus comprising separate read and write paths, said read/write port comprising a single port having a read channel operable to read data from said read path and a write channel operable to write data to said write path, such that data transfers from said data source to said read channel

are received from said read path and data transfers to said data destination are output to said write path independently of said read path.

8. *(Original)* A direct memory access controller according to claim 1, said read/write port further comprising a control channel operable to output control signals to a control path on said bus, said direct memory access controller further comprising:

control logic, said control logic being operable to generate at least one of the following control signals:

a source control signal specifying at least one data transfer from said data source, said control channel of said read/write port being operable to output said source control signal to said data source via said control path on said bus prior to receiving said received data; and

a destination control signal specifying said at least one data transfer to said data destination, said control channel of said read/write port being operable to output said destination control signal to said data destination via said control path on said bus independently of whether said received data has been received at said read/write port.

9. *(Original)* A direct memory access controller according to claim 8, wherein said at least one data transfer comprises a sequence of data transfers from a plurality of consecutive addresses, said control logic being operable to generate single read and write

control signals to respectively control each read and write of said sequence of data transfers from said data source.

10. *(Original)* A direct memory access controller according to claim 9, wherein said single source control signal controls said sequence of data transfers from said plurality of consecutive addresses to be transferred from a central address first, said transfer wrapping round to send data from said initial address following sending data from said final address of said consecutive addresses.

11. *(Original)* A direct memory access controller according to claim 10, said control logic being operable to generate a single destination control signal to control writing of said sequence of data transfers to said data destination.

12. *(Original)* A direct memory access controller according to claim 1, wherein said data source and said data destination each comprise one of either a memory and a peripheral.

13. *(Original)* A direct memory access controller for controlling data transfer between a data source and a data destination comprising:

a single read/write port comprising a read channel operable to receive data from said data source via a read path on a bus and a write channel operable to output said

received data to said data destination via a write path on said bus, said read and write channel being operable to perform data reads and writes independently of each other.

14. *(Original)* A direct memory access controller according to claim 13, said direct memory access controller further comprising control logic, said control logic being operable:

to generate a source control signal specifying at least one data transfer from said data source, said read/write port further comprising a control channel, operable to output control signals along a control path of said bus, said control channel being operable to output said source control signal to said data source prior to receiving said received data at said read channel; and

to generate a destination control signal specifying said at least one data transfer to said data destination, said control channel being operable to output said destination control signal to said data destination independently of whether said received data has been received at said read channel.

15. *(Original)* A direct memory access controller according to claim 13, wherein said at least one data transfer comprises a sequence of data transfers from a plurality of consecutive addresses, said control logic being operable to generate a single source control signal to control sending of said sequence of data transfers from said data source.

16. *(Original)* A direct memory access controller according to claim 15, said control logic being operable to generate a single destination control signal to control writing of said sequence of data transfers to said data destination.

17. *(Original)* A direct memory access control method for controlling data transfer between a data source and a data destination comprising the steps of:

receiving data from said data source via a source bus at a read/write port;

detecting a predetermined number of clock pulses;

in response to said detected predetermined number of clock pulses, controlling said read/write port to output said received data to said data destination via a destination bus said predetermined number of clock pulses after having received it.

18. *(Original)* A direct memory access control method according to claim 17, wherein said predetermined number of clock pulses is one and said method comprises the further step of storing said received data in a register during said one clock cycle prior to outputting it.

19. *(Original)* A direct memory access control method according to claim 17, wherein said predetermined number of clock pulses is one and said received data comprises n data items, said method comprising the further steps of:

(i) storing a first data item of said received data in one of two registers arranged in parallel during one clock cycle;

(ii) outputting said data item stored during said previous clock cycle from one of said two registers and storing a further data item in said other of said two registers during a subsequent clock cycle, wherein step (ii) is performed n –1 times, and

(iii) outputting the last data item of stored data during a further subsequent clock cycle.

20. *(Original)* A direct memory access control method according to claim 17, wherein said predetermined number of clock pulses is zero, and said read/write port is controlled to output said received data after having received it, without storing it.

21. *(Original)* A direct memory access control method according to claim 17, wherein said predetermined number of clock pulses is two and said method comprises the further step of storing said received data in an input register during one clock cycle and storing said received data in an output register during a subsequent clock cycle prior to outputting it.

22. *(Original)* A direct memory access control method according to claim 17, wherein said source bus and said destination bus comprise a single bus, said single bus comprising separate read and write paths, said read/write port comprising a single port

having a read channel operable to read data from said read path and a write channel operable to write data to said write path, said method controlling said read channel to receive data transfers from said data source via said read path, and controlling said write channel to output said received data to said data destination via said write path independently of said read path.

23. *(Original)* A direct memory access control method according to claim 17, said method comprising the further step of generating at least one of the following control signals:

a source control signal specifying at least one data transfer from said data source and controlling a control channel of said read/write port to output said source control signal to said data source via a control path on said bus prior to receiving said received data; and

a destination control signal specifying said at least one data transfer to said data destination, and controlling a control channel of said read/write port to output said destination control signal to said data destination via said control path on said bus independently of whether said received data has been received at said read/write port.

24. *(Original)* A direct memory access control method according to claim 23, wherein said at least one data transfer comprises a sequence of data transfers from a

plurality of consecutive addresses, said method generating a single source control signal to control sending of said sequence of data transfers from said data source.

25. *(Original)* A direct memory access control method according to claim 24, wherein said single source control signal controls said sequence of data transfers from said plurality of consecutive addresses to be transferred from a central address first, said transfer wrapping round to send data from said initial address following sending data from said final address of said consecutive addresses.

26. *(Original)* A direct memory access control method according to claim 24, said method generating a single destination control signal to control writing of said sequence of data transfers to said data destination.

27. *(Original)* A direct memory access control method according to claim 17, wherein said data source and said data destination each comprise one of either a memory and a peripheral.

28. *(Original)* A direct memory access control method for controlling data transfer between a data source and a data destination comprising the steps of:

receiving at a read channel of a single read/write port data from said data source via a read path on a bus; and

outputting said received data from a write channel of said single read/write port to said data destination via a write path on said bus; wherein

said read and write channel perform data reads and writes independently of each other.

29. *(Original)* A direct memory access control method according to claim 28, said method further comprising the steps of:

generating a source control signal specifying at least one data transfer from said data source and controlling a control channel of said read/write port to output said source control signal to said data source via a control path on said bus prior to receiving said received data; and

generating a destination control signal specifying said at least one data transfer to said data destination, and controlling a control channel of said read/write port to output said destination control signal to said data destination via said control path on said bus independently of whether said received data has been received at said read/write port.

30. *(Original)* A direct memory access control method according to claim 29, wherein said at least one data transfer comprises a sequence of data transfers from a plurality of consecutive addresses, said method generating a single source control signal to control sending of said sequence of data transfers from said data source.

31. *(Original)* A direct memory access control method according to claim 30, said method generating a single destination control signal to control writing of said sequence of data transfers to said data destination.

32. *(Currently Amended)* A computer program product, which is operable when run on a data processor to control the data processor to perform the steps of the method according to ~~any one of claims 17 to 31~~claim 17.